Surface Structure of As-modified Si(100) prepared in MOCVD Ambient

P. Kleinschmidt[1], A. Paszuk[1], M. Nandy[1], O. Supplie[1], and T. Hannappel[1]

[1]*Institute of Physics, Technische Universität Ilmenau, Gustav-Kirchhoff-Straße 5, 98693 Ilmenau, Germany*

peter.kleinschmidt@tu-ilmenau.de

Combining III-V materials with group IV semiconductors is desirable for a range of optoelectronic applications, e.g. photovoltaics or solar water splitting. One of the challenges encountered is related to the basic difficulty of growing the polar III-V material on a non-polar substrate, leading to the requirement of a double-layer stepped group-IV substrate in order to avoid anti-phase domains and the associated anti-phase boundaries which form planar defects in the III-V material. This topic has been addressed successfully in the past for both UHV-prepared substrates as well as for substrate preparation in metalorganic chemical vapor deposition (MOCVD) environment employing pure H_2 ambient. Different processing requirements apply in dependence on the offcut and the desired orientation of the surface lattice unit cell (i.e. the orientation of the surface dimers) with respect to the step edges at the surfaces (usually referred to as A-type and B-type or (1×2) and (2×1)) [1]. However, when heteroepitaxy on such substrates is performed in an MOCVD system, group-III and group-V residuals are commonly present in the MOCVD reactor, depending on previous processes. It is therefore highly desirable to investigate the interaction of such residuals with the silicon surface and to find conditions where their presence does not impede subsequent III-V growth, or may even be beneficial to relax substrate process requirements such as high process temperatures.

In this paper we investigate the preparation of Si(100) in arsenic-containing MOCVD environment, where the As can be supplied either directly via the TBAs precursor or as background As_x originating from the reactor walls and the susceptor. The process is controlled in situ by reflection anisotropy spectroscopy (RAS), which is benchmarked to UHV-based surface analytics, thus allowing to specifically prepare Si(100):As surfaces with either (1×2) or (2×1) majority domains. In analogy to the As-free Si(100) surface, the process conditions for achieving preparation of double-layer stepped surfaces of either type differ for lower and higher offcuts. In particular we demonstrate Si(100):As surfaces with 0.1° offcut towards [011] with evenly spaced double layer steps, evidenced by AFM measurement. However, STM investigation of this surface detects the presence of the minority domain, which extends from the double layer step edges onto the adjacent lower majority domain terrace. Additionally, STM results indicate non-symmetric dimers and intermixing of As with Si near the surface.

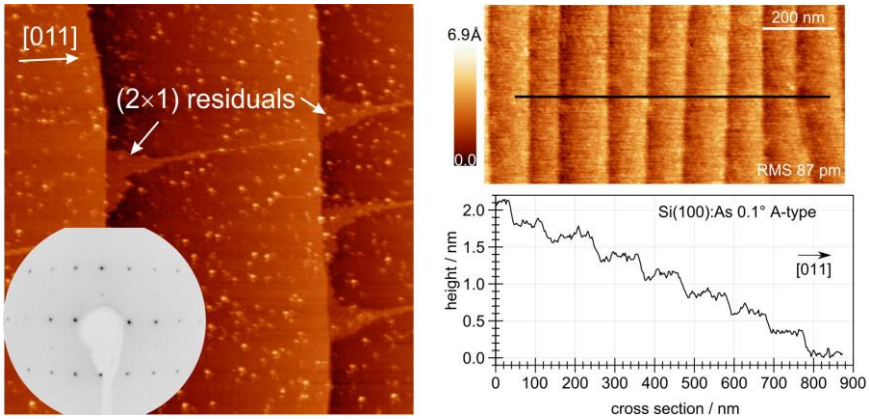

Figure 1: STM, LEED (left) and AFM measurements (right) of 0.1 misoriented Si(100):As, showing A-type double layer steps and the associated predominantly (1×2) reconstructed surface with small (2×1) minority domain residuals.

[1] Brückner, S., Supplie, O., Dobrich, A., Kleinschmidt, P. and Hannappel, T., Phys. Status Solidi B, 1700493 (2017).